Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 11, 17, 23, 30, and 33, and add new claims 35-60, as follows:

Listing of Claims:

1. (Original) A memory hub for a hub-based memory sub-system, comprising:

a high-speed interface for receiving memory access requests;

a non-volatile memory having memory configuration information stored therein; and

a memory controller coupled to the high-speed interface and the non-volatile memory and having registers into which the memory configuration information is loaded, the memory controller operable to output memory requests in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information loaded in the registers.

2. (Original) The memory hub of claim 1 wherein the non-volatile memory comprises an embedded memory integrated with the memory controller.

3. (Original) The memory hub of claim 2 wherein the non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

4. (Original) The memory hub of claim 1, further comprising a local serial bus coupled to the high-speed interface, the non-volatile memory and the memory controller, through which a host system can access the non-volatile memory.

5. (Original) The memory hub of claim 1 wherein the non-volatile memory is further coupled to the high-speed interface.

6. (Original) A memory sub-system for a host computer system, comprising:

a high-speed bus coupled to the host computer system; and

at least one memory module, each memory module having a plurality of memory devices and further having a memory hub coupled to the high-speed link and the plurality of memory devices to control access to the memory devices, the memory hub including a memory controller coupled to the plurality of memory devices of the memory module to output memory access requests to the plurality of memory devices and further including a configuration memory coupled to the memory controller to provide the memory controller with memory module configuration information stored in the configuration memory.

7. (Original) The memory sub-system of claim 6 wherein the configuration memory comprises an embedded non-volatile memory integrated with the memory controller.

8. (Original) The memory sub-system of claim 7 wherein the non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

9. (Original) The memory sub-system of claim 6 wherein the memory hub further comprises a local serial bus coupled to the configuration memory and the memory controller through which the host computer system can access the configuration memory.

10. (Original) The memory sub-system of claim 6 wherein the memory hub further comprises a high-speed interface coupled to the high-speed bus and the memory controller to provide access to the memory module by the host computer system.

11. (Currently amended) The memory sub-system of claim 6 wherein the memory module configuration information <u>at least one of</u> [[is]] timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, <u>and</u> [[or]] manufacturer data.

12. (Original) The memory sub-system of claim 6 wherein the plurality of memory devices of the memory module comprises synchronous dynamic random access memory devices.

13. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub having a high-speed interface for receiving memory access requests, a non-volatile memory having memory configuration information for the plurality of memory devices stored therein, and further having a memory controller coupled to the high-speed interface and the non-volatile memory to output memory requests to the plurality of memory devices in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information stored by the non-volatile memory.

14. (Original) The memory module of claim 13 wherein the non-volatile memory comprises an embedded non-volatile memory integrated with the memory controller and the high-speed interface.

15. (Original) The memory module of claim 14 wherein the non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

16. (Original) The memory module of claim 13 wherein the memory hub further comprises a local serial bus coupled to the non-volatile memory, the high-speed interface, and the memory controller through which a host computer system can access the non-volatile memory.

17. (Currently amended) The memory module of claim 13 wherein the memory configuration information comprises at least one of [[is]] timing information for the

plurality of memory devices of the memory module, memory module configuration data, memory device type, and [[or]] manufacturer data.

18. (Original) The memory module of claim 13 wherein the plurality of memory devices comprises synchronous dynamic random access memory devices.

19. (Original) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

an input/output channel coupled to the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, comprising:

a high-speed interface for receiving memory access requests from the system controller;

a non-volatile memory having memory configuration information for the plurality of memory devices stored therein; and

a memory controller coupled to the high-speed interface and the non-volatile memory to output memory requests to the plurality of memory devices in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information stored by the non-volatile memory.

20. (Original) The processor-based system of claim 19 wherein the non-volatile memory of the memory hub comprises an embedded non-volatile memory integrated with the memory controller and the high-speed interface.

21. (Original) The processor-based system of claim 20 wherein the non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

22. (Original) The processor-based system of claim 19 wherein the memory hub of the memory module further comprises a local serial bus coupled to the non-volatile memory, the high-speed interface, and the memory controller through which the system controller can access the non-volatile memory.

23. (Currently amended) The processor-based system of claim 19 wherein the memory configuration information comprises at least one of [[is]] timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and [[or]] manufacturer data.

24. (Original) The processor-based system of claim 19 wherein the plurality of memory devices comprises synchronous dynamic random access memory devices.

25. (Original) A method for configuring a memory sub-system, comprising:

accessing a plurality of non-volatile memories storing respective configuration information; and

copying the configuration information from each of the plurality of non-volatile memories into configuration registers of a respective one of a corresponding plurality of memory controllers.

26. (Original) The method of claim 25, further comprising providing the respective configuration information from the plurality of non-volatile memories to registers of a system memory controller to which each of the plurality of non-volatile memories is coupled.

27. (Original) The method of claim 26 wherein providing the respective configuration information to registers of a system memory controller comprises coupling the respective configuration information to a serial bus to which the system memory controller is coupled.

28. (Original) The method of claim 25 wherein accessing a plurality of non-volatile memory comprises accessing a plurality of electrically erasable programmable read-only memory.

29. (Original) The method of claim 25 wherein accessing a plurality of non-volatile memory comprises accessing a plurality of embedded non-volatile memories.

30. (Currently amended) The method of claim 25 wherein copying the configuration information comprises copying at least one of timing information for a plurality of memory devices of a memory module, memory module configuration data, memory device type, and [[or]] manufacturer data.

31. (Original) A method for initializing a memory sub-system, comprising:

loading configuration registers of a plurality of memory hubs with the configuration information provided by a respective one of a plurality of embedded non-volatile memories integrated in the respective memory hub.

32. (Original) The method of claim 31, further comprising providing the configuration information from the plurality of embedded non-volatile memories to registers of a system memory controller to which each of the plurality of embedded non-volatile memories are coupled.

33. (Currently amended) The method of claim 31 wherein loading configuration registers of a plurality of memory hubs with the configuration information

comprises loading configuration registers of the plurality of memory hubs with at least one of timing information for a plurality of memory devices of a memory module on which the respective memory hub is located, memory module configuration data, memory device type, and [[or]] manufacturer data.

34. (Original) The method of claim 31 wherein loading configuration registers of a plurality of memory hubs comprises loading configuration registers of a memory controller integrated in a respective one of the plurality of memory hubs.

35. (New) A memory hub for a hub-based memory sub-system, comprising:

a high-speed interface for receiving memory access requests;

an electrically programmable non-volatile memory having memory module configuration information stored therein; and

a memory controller coupled to the high-speed interface and the electrically programmable non-volatile memory and having registers into which the memory configuration information is loaded, the memory controller operable to output memory requests in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information loaded in the registers.

36. (New) The memory hub of claim 35 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

37. (New) The memory hub of claim 35, further comprising a local serial bus coupled to the high-speed interface, the electrically programmable non-volatile memory and the memory controller, through which a host system can access the electrically programmable non-volatile memory.

38. (New) A memory sub-system for a host computer system, comprising:

a high-speed bus coupled to the host computer system; and

at least one memory module, each memory module having a plurality of memory devices and further having a memory hub coupled to the high-speed link and the plurality of memory devices to control access to the memory devices, the memory hub including a memory controller coupled to the plurality of memory devices of the memory module to output memory access requests to the plurality of memory devices and further including a configuration memory coupled to the memory controller to provide the memory controller with memory module configuration information stored in the configuration memory and to store memory module configuration information written to the configuration memory.

39. (New) The memory sub-system of claim 38 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

40. (New) The memory sub-system of claim 38 wherein the memory hub further comprises a local serial bus coupled to the configuration memory and the memory controller through which the host computer system can access the configuration memory.

41. (New) The memory sub-system of claim 38 wherein the memory hub further comprises a high-speed interface coupled to the high-speed bus and the memory controller to provide access to the memory module by the host computer system.

42. (New) The memory sub-system of claim 38 wherein the memory module configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

43. (New) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub having a high-speed interface for receiving memory access requests, an electrically erasable programmable non-volatile memory having memory configuration information for the plurality of memory devices stored therein, and further having a memory controller coupled to the high-speed interface and the electrically erasable programmable non-volatile memory to output memory requests to the plurality of memory devices in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information stored by the electrically erasable programmable non-volatile memory.

44. (New) The memory module of claim 43 wherein the electrically erasable programmable non-volatile memory comprises an embedded non-volatile memory integrated with the memory controller and the high-speed interface.

45. (New) The memory module of claim 43 wherein the memory hub further comprises a local serial bus coupled to the electrically erasable programmable non-volatile memory, the high-speed interface, and the memory controller through which a host computer system can access the electrically programmable non-volatile memory.

46. (New) The memory module of claim 43 wherein the memory configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

47. (New) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

an input/output channel coupled to the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, comprising:

a high-speed interface for receiving memory access requests from the system controller;

an electrically programmable non-volatile memory having memory module configuration information for the plurality of memory devices stored therein; and

a memory controller coupled to the high-speed interface and the electrically programmable non-volatile memory to output memory requests to the plurality of memory devices in response to receiving memory access requests from the high-speed interface and in accordance with the memory configuration information stored by the electrically programmable non-volatile memory.

48. (New) The processor-based system of claim 47 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

49. (New) The processor-based system of claim 47 wherein the memory hub of the memory module further comprises a local serial bus coupled to the electrically programmable non-volatile memory, the high-speed interface, and the memory controller through which the system controller can access the electrically programmable non-volatile memory.

50. (New) The processor-based system of claim 47 wherein the memory configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

51. (New) A method for configuring a memory sub-system having at least one memory module having a plurality of memory devices, the method comprising:

accessing a plurality of electrically programmable non-volatile memories storing respective configuration information including at least one of timing information for memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data; and

copying the configuration information from each of the plurality of electrically programmable non-volatile memories into configuration registers of a respective one of a corresponding plurality of memory controllers.

52. (New) The method of claim 51, further comprising providing the respective configuration information from the plurality of electrically programmable non-volatile memories to registers of a system memory controller to which each of the plurality of electrically programmable non-volatile memories is coupled.

53. (New) The method of claim 52 wherein providing the respective configuration information to registers of a system memory controller comprises coupling the respective configuration information to a serial bus to which the system memory controller is coupled.

54. (New) The method of claim 52 wherein accessing a plurality of electrically programmable non-volatile memory comprises accessing a plurality of electrically erasable programmable read-only memory.

55. (New) The method of claim 52 wherein accessing a plurality of electrically programmable non-volatile memory comprises accessing a plurality of embedded non-volatile memories.

56. (New) The method of claim 52 wherein copying the configuration information comprises copying at least one of timing information for a plurality of memory devices of a memory module, memory module configuration data, memory device type, and manufacturer data.

57. (New) A method for initializing a memory sub-system having at least one memory module having a plurality of memory devices, the method comprising:

loading configuration registers of a plurality of memory hubs with the configuration information including at least one of timing information for memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data, the configuration information provided by a respective one of a plurality of embedded electrically programmable non-volatile memories integrated in the respective memory hub.

58. (New) The method of claim 57, further comprising providing the configuration information from the plurality of embedded electrically programmable non-volatile memories to registers of a system memory controller to which each of the plurality of embedded electrically programmable non-volatile memories are coupled.

59. (New) The method of claim 57 wherein loading configuration registers of a plurality of memory hubs with the configuration information comprises loading configuration registers of the plurality of memory hubs with at least one of memory module capacity and memory module clock speed.

60. (New) The method of claim 57 wherein loading configuration registers of a plurality of memory hubs comprises loading configuration registers of a memory controller integrated in a respective one of the plurality of memory hubs.